

1        1. (Three Times Amended) A method comprising:

2                 providing a plurality of memory banks of semiconductor memory devices,  
3                 each memory bank being accessible to first and second processors for operations  
4                 selected from the group comprising read and write operations; and

5                 storing subsets of audio data from a plurality of audio channels in the  
6                 plurality of memory banks, the subsets corresponding to different groups of the  
7                 audio channels.

1        2. (Amended) The method of claim 1, further comprising selecting said  
2         memory banks for access by one of the first and second processors.

1        3. (Twice Amended) The method of claim 1 wherein the plurality of memory  
2         banks includes two memory banks.

1        4. The method of claim 3 wherein one subset of said audio data corresponds to  
2         even-numbered audio channels and one other subset of said audio data corresponds to odd-  
3         numbered audio channels.

1        5. (Three Times Amended) A system comprising:  
2                 first and second buses;

3           a first processor and a second processor coupled to said first and second busses,  
4       respectively; and

5           a plurality of memory banks of semiconductor memory devices coupled to said first  
6       and second buses for storing said audio data, said plurality of memory banks being  
7       accessible to the first and second processors for operations selected from the group  
8       comprising read and write operations, said plurality of memory banks storing subsets of  
9       audio data from a plurality of audio channels, said subsets corresponding to different  
10      groups of the audio channels.

1           6.       (Amended) The system of claim 5 further comprises a plurality of selectors  
2       coupled said first and second busses to select said memory banks for access by one of said  
3       first and second processors.

1           7.       (Amended) The system of claim 6 wherein the plurality of selectors include  
2       a plurality of address multiplexers and data transceivers.

1           8.       The system of claim 5 wherein one subset of said audio data corresponds to  
2       even-numbered audio channels and one other subset of said audio data corresponds to odd-  
3       numbered audio channels.

1           9.       (Amended) The system of claims 5, wherein the memory banks include  
2       dynamic random access memories.

1           10. The method of claim 1, wherein storing further comprises interleaving the  
2 subsets of data.

1           11. The system as set forth in claim 5, wherein the subsets are stored in the  
2 memory banks in an interleaving manner.

1           12. The method of claim 1, wherein storing comprises storing one of the subsets  
2 of audio data in one of the memory banks, said method further comprising reading stored  
3 audio data from a second of the memory banks.

1           13. The method as set forth in claim 1, wherein the first processor performs a  
2 read operation on a first memory bank of the plurality of memory banks and the second  
3 processor performs a write operation on a second memory bank of the plurality of memory  
4 banks.

1           14. The system of claim 5, wherein subsets of audio data are stored in one of the  
2 memory banks and stored audio data is read from a second of the memory banks.

1           15. The system as set forth in claim 5, wherein the first processor performs a  
2 read operation on a first memory bank of the plurality of memory banks and the second  
3 processor performs a write operation on a second memory bank of the plurality of memory  
4 banks.